



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,121	01/15/2002	Brian Keith Owens	2001-0273.00	1297

21972 7590 11/17/2006

LEXMARK INTERNATIONAL, INC.
INTELLECTUAL PROPERTY LAW DEPARTMENT
740 WEST NEW CIRCLE ROAD
BLDG. 082-1
LEXINGTON, KY 40550-0999

EXAMINER

KANG, ROBERT N


ART UNIT

PAPER NUMBER

2625

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/047,121	Applicant(s) OWENS ET AL.	
	Examiner Robert N. Kang	Art Unit 2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 August 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6, 12 and 14-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14-18 is/are allowed.
- 6) ☒ Claim(s) 12 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

Response to Arguments

1. Applicant's arguments, see page 5 of Applicant's response, filed 8/29/2006, with respect to the rejection(s) of claim(s) 6 and 12 under 35 U.S.C. 102(b) and 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hirota (US 6,606,707).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Hirota (US 6,606,707).

Hirota discloses a semiconductor memory card 109, which is typically flash memory 331 including a ROM 304. The interface pins shown in FIG. 5 are analogous to the "serial flash to ROM interface" 18 of the applicant's disclosure, as it connects a bank of read-only-memory cells via an interface generally reserved for flash memory.

Examiner further cites products such as the HP 39594F#4350 compact-flash card and various other Read Only Memories coupled through a Flash interface. Therefore Hirota anticipates limitations a and b, 3 (EPROM to ROM), and 4 (Flash to ROM).

Additionally, Hirota depicts in FIG. 13 a memory addressing mode wherein each consecutive block is numbered with a 4-bit physical address. Therefore, the data is read from data pins DATA1-DATA4 in consecutive words, i.e., serially. Thus the "Flash to ROM interface is a serial interface."

Furthermore, Hirota in FIG. 5 depicts a CLOCK input pin, 4 data pins, which comprise "serial input transmission lines and serial output transmission lines" based upon the instruction sent to the COMMAND pin, and a special area access control unit 324, connected through the command judgment control unit 322, which accesses the ROM. This therefore comprises a "chip select line." Finally, the "write" command, when utilized to write all 0's, is functionally equivalent to a "reset transmission line" and inherent in all memory media.

Hirota discloses, "the command judgment control unit 322 is a controller composed of a decoding circuit and control circuit. The decoding circuit identifies a command (an instruction to the memory card 109) input via a command pin and executes the identified command... the commands received... includes not only commands to read, write, and delete data from/into the flash memory 303, but commands to control the flash memory 303 (commands related to an address space, not-deleted data, etc.)" (col. 10 line 66- col. 11 line 10). Therefore, a transmitted command includes the group "status, read, and write."

Finally, Hirota states in column 12, "the special area 304 is a read-only area. A dedicated command is used to read data from the special area 304." Thus, the "Flash to ROM interface executes the read command with respect to the ROM memory cells but cannot update the data stored in the ROM memory cells."

3. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima (US-PAT 6,250,827) in view of (US 6,606,707).

Regarding limitation 1, Nojima discloses in paragraph (249), "In FIG. 45, reference numeral 500 designates an ASIC in which the MPU part and printer control part are integrated. Numeral 504 represents a flash ROM which stores programs for controlling the whole of the recording device, numeral 505 a mask ROM storing character fonts etc., and numeral 506 a DRAM used as a work area of the ASIC 500 and as a buffer of signal. Numeral 509 denotes an EEPROM, this EEPROM 509 being a rewritable ROM which can retain the contents without supply of power." Therefore Nojima's invention qualifies as "a printer-controller ASIC having non-ROM memory control."

Nojima does not disclose a "memory module including ROM memory cells and a non-ROM to ROM interface operatively connected to the ROM memory cells, and a transmission cable operatively connected to the non-ROM memory control of the printer controller ASIC and the non-ROM to ROM interface of the memory module."

Hirota discloses a memory module which meets the limitations of claim 6.

Nojima and Hirota are combinable because they both deal with ROM memory management in low cost devices such as printer ASICs and audio players.

It would have been obvious at the time of invention to one of normal skill in the art to implement in Nojima's printing system Hirota's memory module by replacing the DSP with the printer ASIC in the memory module block diagram. Furthermore, updating fonts and firmware through a read-only Flash memory was well-known at the time of invention.

The motivation of this modification would be to allow easy debugging and changes to the internal program memory of the print ASIC through the Flash Memory. Therefore it would have been obvious to combine Nojima and Hirota to achieve the invention of claim 12.

Allowable Subject Matter

4. Claims 14-18 are allowed.

5. The following is an examiner's statement of reasons for allowance: claim 14 under limitation b, line 5, states "the second memory module physically replaces the first memory module." Examiner can find no prior art of record wherein a finalized version of code is stored in a ROM and physically replaces the non-ROM memory which contained a non-final version of the development code, particularly in the context of a printer ASIC.

Several well-known examples of upgrading firmware utilize physically replacing a ROM or PROM with an identical unit having newer software contained thereon. However, replacing an EPROM with a ROM is typically unfounded in the art.

Additionally, the non-ROM to ROM interface disclosed in memory module 10 can be found in numerous applications, such as the HP 39594F#4350 compact-flash card, which includes a PDL or firmware on a ROM. A compact-flash card is well known as a writable memory, and thus the interface between the card and the ROM of the memory module is well known. However, none of the relevant prior art of record indicates that this ROM physically replaces an EPROM containing the non-final version of program firmware.

Finally, classes 714/6, 365/185.29, and 365/185.33 contain numerous patents on implementing memory redundancy, wherein a physical block (meaning a contiguous region of a memory i.e., a section of circuits or switches) of memory replaces another physical block of memory due to failure or defect. However, these inventions generally pertain to a redundancy circuit wherein a logical replacement for physical blocks of memory is carried out; numerous references in this class specifically make the distinction between physical and logical replacement of memory.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

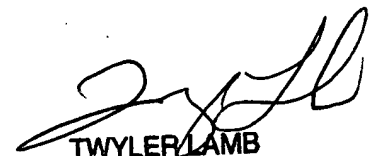
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert N. Kang whose telephone number is 571-272-0593. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler M. Lamb can be reached on (571)272-7406. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



RNK



TWYLER LAMB
SUPERVISORY PATENT EXAMINER